Comparative Investigation on Numerical De-Embedding Techniques for Equivalent Circuit Modeling of Lumped and Distributed Microstrip Circuits

Lei Zhu, *Senior Member, IEEE*, and Ke Wu, *Fellow, IEEE*

***Abstract*—A so-called "short-open calibration" (SOC) technique is applied together with two existing numerical de-embedding techniques for equivalent circuit modeling of microstrip circuits based on a full-wave method-of-moments (MoM) algorithm. A stub-loaded microstrip line discontinuity with both electrically short (lumped) and long (distributed) stub lengths is extensively studied in terms of its Z-matrix circuit model. Our obtained results show that the SOC scheme allows an accurate calibration of all the potential error terms out of the core circuit network, thereby avoiding numerical noise-related behaviors regardless of either lumped or distributed circuits, which are nevertheless observed for the two existing techniques.**

***Index Terms*—Equivalent circuit model, lumped and distributed microstrip circuits, method of moments (MoM), short-open calibration (SOC) technique.**

I. INTRODUCTION

OVER the past decades, three-dimensional (3-D) full-wave method of moments (MoM) algorithms [1]–[5] have widely been studied for numerical characterization of planar integrated circuits and antennas, which have generated a number of commercial packages. They have successfully been used for direct field-based design and optimization of complex planar integrated circuits by undertaking time-consuming iterative simulations that are often concerned with electrically large structures. Generally, the circuit designer prefers to partition the whole structure into a number of electrically small elements, characterize them in terms of their corresponding equivalent circuit models, and then carry out the final design procedure based on a well-developed network approach. Indisputable accuracy of S-parameter simulations for electrically large (distributed) planar circuits is usually expected, such as resonator-type filters. However, work has been reported, but few to de-embed or extract the equivalent circuit models of electrically small (lumped) planar elements from the field-theoretical MoM simulations.

To our knowledge, there exist parasitic error terms in the source-type or deterministic MoM algorithms [1]–[5]. They are attributed by the approximate introduction of excitation models at the external ports or terminal and also inconsistency of two dimensional (2-D) and 3-D MoM modeling of finitely extended feed lines between the source port and the reference plane of choice [6], [7]. In [7], a so-called "short-open calibration" (SOC) technique was originated and proposed to evaluate and remove out such error terms through the definition of two perfect calibration standards in the 3-D MoM, namely, *short* and *open circuits*. In this work, this SOC scheme is applied in our MoM scheme [5] together with the two existing techniques based on the transmission line theorem for numerical de-embedding of a stub-loaded microstrip line with both electrically short (lumped) and long (distributed) stub lengths. Our obtained results not only confirm the effectiveness and accurateness of our SOC technique, but also show, for the first time, the adversary nature of these error terms in de-embedded network parameters of the lumped and distributed microstrip circuits.

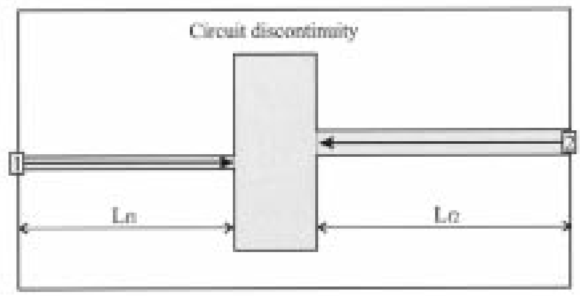

Fig. 1. Physical layout for the 3-D MoM modeling of a two-port stub-loaded microstrip line discontinuity.

II. SOC DE-EMBEDDING TECHNIQUE

Fig. 1 describes a physical layout arranged for the full-wave MoM modeling of a stub-loaded microstrip line discontinuity having two external feed lines driven by impressed electric fields or voltage sources at the two ports as well as numerical de-embedding scheme of the core equivalent circuit model at two reference planes of the discontinuity, e.g., two step interfaces. As explained in [5], this admittance-type MoM algorithm allows a direct characterization of the two-ports Y- or Z-matrix circuit network at the two source ports on the basis of the fact that the electric currents flowing at these two ports can explicitly be determined as a function of the two port voltages. The key issue of our concern here is how to effectively de-embed or extract this core circuit network at the interfaces

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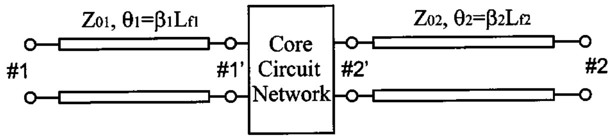
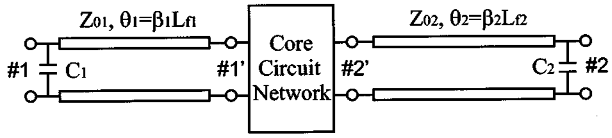


(a)



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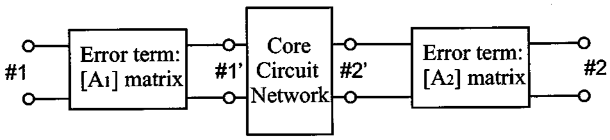


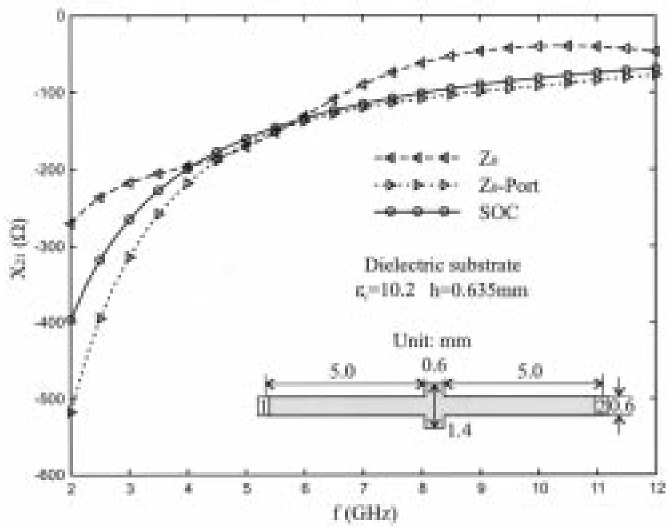
(c)

Fig. 2. Equivalent network topology arranged for the de-embedding of a two-port stub-loaded microstrip line discontinuity using our SOC and the two existing techniques. (a) Z_0 technique; (b) Z_0-port technique; (c) SOC technique.

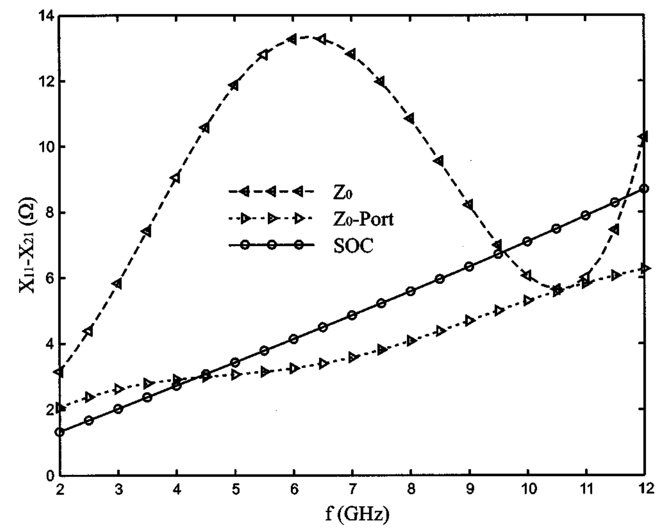
of the two strip steps along this discontinuity. This circuit network is very useful for CAD synthesis and optimization of planar passive and active integrated circuits.

Fig. 2(a) describes the equivalent circuit representation of the conventional de-embedding technique based on the ideal transmission line theorem, called "Z_0 *technique*," which completely ignores the two aspects of error mentioned above. As indicated in Fig. 2(a), the two microstrip feed lines of lengths L_{f1} and L_{f2} are perceived as two ideal transmission lines modeled with characteristic impedance (Z_0) and effective dielectric constant (ε_{re}), which are obtained from the 2-D MoM modeling of an infinitely long uniform microstrip line. This simple technique is found appropriate in the de-embedding of electrically large (distributed) planar integrated circuits such as resonator-type filters, but fails to handle electrically small (lumped) planar circuits such as simple microstrip open circuits as explained in [7]. Fig. 2(b) describes an improved transmission-line-based de-embedding procedure called "Z_0-*Port technique*" in this work. In this case, each port discontinuity is modeled as a lumped shunt capacitance and its value here is found about 0.108 pF at low frequency. The two feed lines are still considered as the two ideal transmission lines as before.

Fig. 2(c) shows the equivalent circuit representation using our SOC de-embedding technique [7], in which the complete network topology of the two-port discontinuity is divided into three distinct parts: core circuit network and two error terms. Each error term represents the whole electrical behavior of its corresponding feed line driven by the impressed source, including the approximate effect of the excitation model and the inconsistency effect of 2-D and 3-D MoM modeling of this microstrip feed line. In this scheme [7], a pair of calibration standards (*short* and *open circuits*) can be defined in the 3-D MoM as the microstrip line section of the same length as its corresponding feed line, which is driven by the impressed source and terminated by perfect short-/open-ends or electric/magnetic walls. Such SOC standards are formulated to evaluate the circuit network parameters of the error terms and eventually remove them out of the core equivalent network with the use of the complete network topology as in Fig. 2(c).



(a)

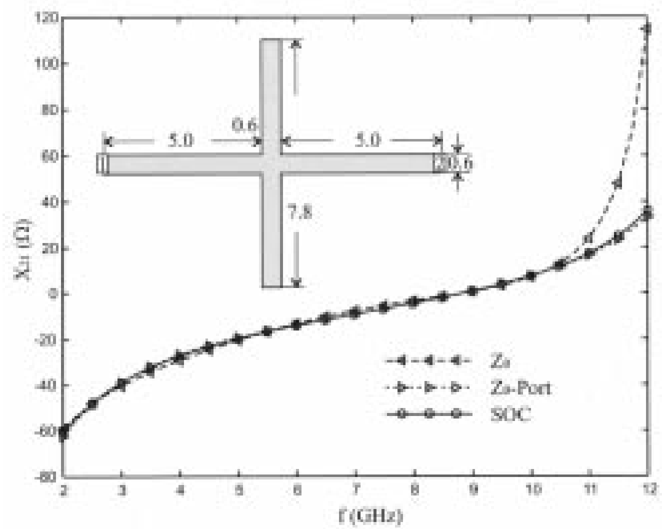


(b)

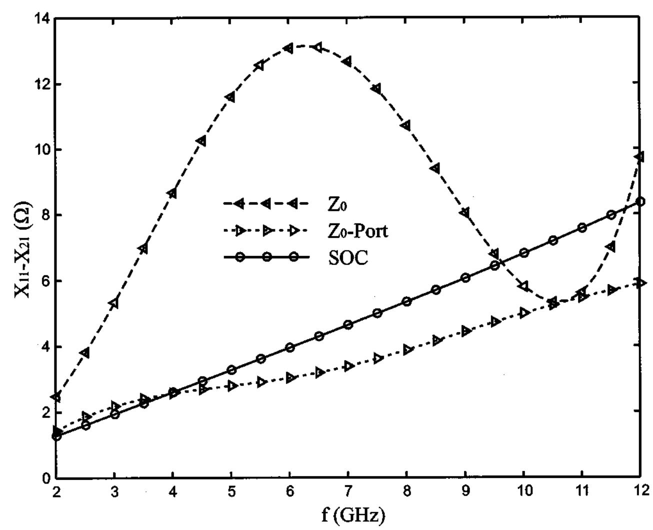
Fig. 3. Comparison among three groups of de-embedded Z-parameters of an electrically short (lumped) stub-loaded microstrip discontinuity using the three de-embedding techniques as in Fig. 2.

III. De-Embedded Parameters of Microstrip Circuits

Let's look at the numerical de-embedding of the core circuit parameters of the stub-loaded microstrip line discontinuity with the three de-embedding techniques. Fig. 3 depicts the de-embedded Z-matrix parameters for the case of a pair of identical short stub lengths (0.4 mm) that correspond to a lumped shunt capacitive circuit. Parameters with mutual-reactance X_{21} and self-reactance $(X_{11}–X_{21})$ represent a single and two shunt reactances of the equivalent T-type circuit model, respectively. First, it is observed that the results of the Z_0 technique appear to be an irregular function of frequency, especially for the parameter $(X_{11}–X_{21})$ in Fig. 3(b). This noise-related numerical instability is generated by the mixed approximation of nonideal excitation model at the ports and the mismatched (or inconsistent) 2-D and 3-D MoM modeling of the feeding lines. Second, the results of the Z_0-*Port* technique indicate that the



(a)



(b)

Fig. 4. Comparison among three groups of de-embedded Z-parameters of an electrically long (distributed) stub-loaded microstrip discontinuity using the three de-embedding techniques as in Fig. 2.

above-observed numerical instability gains a significant reduction due to the effective removal of the port discontinuity. Still, we can see a minor error somehow, such as a nonlinear variation of (X_{11}–X_{21}) with frequency as in Fig. 3(b), which is mainly caused by the inconsistent 2-D and 3-D MoM modeling of the feed lines and also the approximate lumped model of the port discontinuity. In the meantime, the SOC parameters appear smoothly varied as a function of frequency as shown in Fig. 3(c). The SOC-extracted X_{21} always remains negative and goes up with frequency, exhibiting the electrical behavior of shunt capacitance. The SOC-extracted (X_{11}–X_{21}) increases as a perfectly linear function of frequency, which represents the two extremely small series inductances in the afore-mentioned T-type circuit model.

Now, such a pair of stub lengths is extended from 0.4 mm to 3.6 mm in order to make up an electrically large (distributed) microstrip circuit. Fig. 4 gives the relevant de-embedded parameters X_{21} and (X_{11}–X_{21}). We can observe that all the de-embedded X_{21} agree well with each other at frequency lower than 10.0 GHz regardless of the choice of the techniques discussed above and it becomes 0 Ω at $f = 8.8$ GHz due to the resonance of the quarter-wavelength open-end stub. This result provides a quantitative confirmation for our own viewpoint that the numerical errors in the determinant 3-D MoM can completely be ignored if the circuit parameter under de-embedding is strongly frequency distributed or larger than those of the port discontinuity and 2-D/3-D MoM mismatch effects. However, it can be seen from Fig. 4(b) that the parameters (X_{11}–X_{21}) are almost kept the same as those in Fig. 3(b), exhibiting that the de-embedded lumped parameters from the two former techniques still present a numerically instable problem due to their values comparable to those of numerical error terms. By contrast, the SOC-extracted parameters (X_{11}–X_{21}) show a good linear function of frequency as in Fig. 3(b), again verifying that this scheme has an excellent capacity in calibration of all the numerical errors out of the core circuit model under de-embedding.

IV. CONCLUSIONS

The SOC technique is applied jointly with the two existing techniques for the numerical de-embedding or extraction of equivalent circuit network of a stub-loaded microstrip line discontinuity with short and long stubs in connection with lumped and distributed circuits, respectively. The results give a clear evidence of the effectiveness and accurateness of our SOC technique for numerical de-embedding or extraction of equivalent circuit models for both lumped and distributed cases. Also, we demonstrate in a quantitative manner that the existing techniques are limited for de-embedding of equivalent circuit networks for electrically small (lumped) planar circuits due to the intolerable numerical errors in the determinant MoM algorithm.

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